MULTICORE PROCESSORS FOR AVIONICS:

MODELING AND ARCHITECTURAL CHALLENGES

Interview with:

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In the lead-up to IQPC's Multicore Processors for Airborne Systems Conference 2020, Jyotica Athavale addresses the challenges to develop MCP technology. Through a gap analysis between the DO-254 and the Automotive ISO 26262 functional safety standards, avionics safety requirements can be mapped to corresponding artifacts from automotive ISO 26262 certification.

Could you give us an overview of the SOC-related technologies that are being developed for functionally safe avionics?

First, the trend to coordinate network access and to ensure bandwidth guarantees leads towards deployment of Time-Sensitive Network (TSN) approaches instead of traditional avionics networks. Second, given this trend from further integration on single chips, architectures need to evolve to coordinate time and preserve guarantees that typically have been provisioned at system-level (network-level). Intel introduces Time-Coordinated Compute (TCC) to coordinate actions on-chip. The once federated avionics systems are now increasingly interconnected, and software-driven, causing security concerns to grow. Datalink and networking capabilities are bringing additional data to the cockpit. This can cause serious security issues to occur. To address cybersecurity, isolation must also hinder the ability of one partition to infer information about the other.

What challenges are there in terms of modelling and architecture technologies to develop multicore processors for airborne systems?

MCPs are highly-complex SoCs (System-on-Chip) that provide many resources, including processing cores, memory devices and interconnects. Users can tailor the resources to the requirements of their equipment by selecting specific aspects, such as which cores are activated, their execution frequencies, whether shared memory is used and how they are allocated. If these configuration settings of the MCP are inadvertently altered during operation by Single Event Effects or other causes, they could cause the MCP to no longer comply with their requirements. SEU (Single Event Upset) or SEL (Single Event Latchup) are especially of concern given the higher neutron flux at higher altitudes. Mitigating these effects is critical since the transient error requirements are very stringent especially for DAL A and DAL B systems. Modern MCPs are the central component of a complex SoC architecture, where additional resources such as a memory hierarchy, I/O peripherals and an on-chip fabric to interconnect them are shared among multiple co-running applications, as needed.

Unfortunately, non-exclusive usage of system resources comes at the price of runtime interference. Therefore, the raw performance speedup offered by additional execution units is often at odds with the overhead introduced by access arbitration or, worse, execution state reconstruction.

What knowledge can be drawn from the automotive sector to develop avionics SOC tech?

By completing a gap analysis between the DO-254 and the Automotive ISO 26262 functional safety standards, the DO-254 avionics safety requirements can be mapped to corresponding artifacts from automotive ISO 26262 certification, thereby leveraging certification efforts for automotive towards flight safety.

ISO 26262 was published in 2012 for the purpose of providing a comprehensive safety standard for electronic systems contained in passenger road vehicles. The RTCA DO-254 / Eurocae ED-80 document is a set of hardware design assurance guidelines employed in the civil aviation industry for safety-related requirements of a hardware implementation.

The top-level safety processes between the two standards can be considered to be compatible although the terminology and resulting work products are different. It is possible to map between major objectives, requirements, methods, and activities discussed in the two standards although there are significant differences in emphasis and terminology. Work products, data items and lifecycles can be mapped between the two standards. The safety approaches are generally equivalent.

Testing and ISO 26262 compliance are an automotive industry obsession. How would the standard landscape look like should SOCs debut in airborne systems?

The Federal Aviation Administration (FAA) and European Aviation Safety Agency (EASA) worked with industry to quantify a set of requirements and guidance that should be met to certify and use MCPs in civil aviation, described e.g. in the FAA CAST-32A Position Paper and the EASA Use of multicore processors in airborne Systems (MULCORS) research report and assurance of MCP research of FAA. Lately, EASA and FAA have proposed formal guidance with an advisory circular addressing augmentations to ED-80/DO-254. A more general research report of an FAA-sponsored research project describes the issues and emerging solutions for COTS equipment.

What are the requirements for design and innovation that lead to key success?

For avionics to use MCP efficiently, the electronics industry should support with information where feasible, possible, and reasonable. MCPs introduce new instances of potential interaction between applications. Newer devices that incorporate COTS features such as TCC and TSN, have the potential to alleviate certification challenges.
Access to external interfaces increases vulnerability to security attacks.
These threats can also increase risks to flight safety and should be addressed at multiple system levels.

Interview conducted by Cristian Bustos

Jyotica Athavale, Principal Engineer Senior Functional Safety and RAS Architect at Intel Corporation, USA will participate in:

PRESENTATION | SOFT ERROR RATE QUALIFICATION AND RADIATION EFFECTS

Functional Safety and in particular how to achieve compliance to Soft Error Rate requirements is posing many challenges that need to be addressed to be successful in markets such as multicore avionics in airborne systems. This presentation will feature an overview of these technologies and challenges for SOC components, including soft error testing and modeling methodologies, error classification and the use of innovative mitigation strategies in architecture and design to meet the SER needs of the functional safety standards. The presentation also covers TCC (Time Coordinated Computing) efforts to enable CAST32A for flight safety avionics systems.

EXPERT PANEL | CHANGING TO MULTI-CORE

Future of airborne systems The need for better performance and reliability is truly underway and the industry needs to consider the requirements and how they will play a major role for the future aviation architectures.

ROUND TABLE DISCUSSION | TABLE A

Considerations for eVTOL / Urban air mobility?

WORKSHOP D | THE POWER OF DENSE SILICON: TRENDING FEATURES & SUPPORT AT CHIP-LEVEL ENABLING NEW LEVELS OF INTEGRATION AND DEPENDABILITY FOR AVIONICS SYSTEMS

Weight is fuel and cost. In the future the quest to continue integration and leverage modern powerful compute fabrics will continue to be a central goal of modern avionics architectures combined with functional integration to create emergent new functionality. Additionally, cost savings in aerospace lead to the need of having to use commercial-off-the-shelf (COTS) computing architectures. In this talk we describe some current and possibly future trends and then investigate how these trends affect avionics. We describe issues and mitigation techniques introduced due to COTS electronics with focus on multi-core processors (MCP) in avionics architectures and their requirements. We discuss what standards and processes need to be followed and what support from chip vendors (certification package) can help. We also present how new avionics architectures could leverage certain COTS trends driven by industrial control and automotive to help integration and optimization of future avionics architectures.

CHALLENGES WHEN IT COMES TO TECHNOLOGICAL ADVANCEMENTS IN MULTI-CORE

Multi-core Processors for Airborne Systems

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Aircraft avionics are on the brink of perhaps its greatest transformation, with the introduction of multi-core processors. However, issues like interference and the need of new architectures have engineers scratching their heads as to how to find mitigation solutions, write accurate and feasible test cases. How deeply will MCP affect the industry and what are the challenges to unlock the avionics future.